REMARKS

Claims 1 to 19 were pending in the Application at the time of examination. The Examiner rejected Claims 1, 4, 5, 6, 12, 13, 14, 15, 16, 17, 18, and 19 under 35 U.S.C. 102(b) as anticipated by the Irrinki reference (US 6,067,262). The Examiner rejected Claims 2, 3, 7, 8, 9, 10, and 11 under 35 U.S.C. 103(a) as obvious over the Irrinki reference (US 6,067,262) in view of the Dreibelbis et al. reference (US 5,173,906).

Applicants have amended Claim 18 to correct Claim 18's dependency from Claim 18 to the proper Claim 16. Claims 1 to 19 remain in the Application.

REJECTION OF CLAIMS 1, 4, 5, 6, 12, 13, 14, 15, 16, 17, 18, AND 19 BASED ON 35 U.S.C. 102(b)

The Examiner rejected Claims 1, 4, 5, 6, 12, 13, 14, 15, 16, 17, 18, and 19 under 35 U.S.C. 102(b) as anticipated by the Irrinki reference (US 6,067,262).

Applicants' Claim 1 reads as follows, with emphasis added:

> An integrated circuit comprising:
> a plurality of memory arrays;
> **Address Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, wherein the **ASI bus interface logic controls access to the plurality of memory arrays**;
> a memory control unit connected to the **ASI bus interface logic**; and
> a memory built-in self-test (MBIST) engine connected to **the ASI bus interface logic**, wherein the MBIST engine utilizes **the ASI bus interface logic** to perform memory testing on at least one of the plurality of memory arrays.

Applicants' Claim 7 reads as follows, with emphasis added:

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> A memory built-in self-test (MBIST) engine for an integrated circuit having a plurality of memory arrays, **Address Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, and a memory control unit connected to **the ASI bus interface logic**, wherein the MBIST engine utilizes **the ASI bus interface logic** to perform memory testing on at least one of the plurality of memory arrays, the MBIST engine comprising:
>
> a programmable state machine controller;
>
> a programmable data generator connected to the controller, wherein the data generator provides data appropriate for a particular test situation;
>
> a programmable address generator connected to the controller, wherein the address generator provides addresses appropriate for the particular test situation; and
>
> a programmable comparator connected to the controller, wherein the comparator provides test results information for the particular test situation to the controller.

Applicants' Claim 12 reads as follows, with emphasis added:

> A method of memory built-in self-test (MBIST) for an integrated circuit having a plurality of memory arrays, Address **Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, a memory control unit connected to **the ASI bus interface logic**, and an MBIST engine connected to **the ASI bus interface logic**, the method comprising:
>
> utilizing **the ASI bus interface logic** to perform memory testing on at least one of the plurality of memory arrays.

Applicants' Claim 16 reads as follows, with emphasis added:

> An apparatus for memory built-in self-test (MBIST) for an integrated circuit having a plurality

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> of memory arrays, **Address Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, a memory control unit connected to **the ASI bus interface logic**, and an MBIST engine connected to **the ASI bus interface logic**, the apparatus comprising:
>
> means for utilizing the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays.

As shown above, each of Applicants' independent Claims specifically recites, multiple times per claim, an **Address Space Identifier (ASI) bus** and **Address Space Identifier (ASI) bus interface logic.**

These very specific structures are discussed throughout Applicants' Specification. For instance, Applicants paragraph [003] at page 4 of Applicants' Specification reads as follows, with emphasis added:

> Taken together, the memory space of the various memory arrays in the IC can be logically viewed as the complete address space of the IC. The individual memory arrays are then viewed as a logical partition of this unified address space. The individual memory arrays can be identified by their address locations in the unified address space. **One example of such organization, called the Address Space Identifier (ASI) architecture, is provided by the Scalable Processor ARChitecture (SPARC) microprocessor specification. The SPARC specification is an open specification created by the SPARC Architectural Committee of SPARC International.** One can implement a microprocessor chip that is compliant with the SPARC specification by securing a license from SPARC International. The SPARC specification is well known and will serve as the basis of the discussion that follows. However, this is not to be interpreted as meaning that the following discussion is strictly limited to the SPARC specification.

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As another example, Applicants paragraph [005] at pages 5 and 6 of Applicants' Specification reads as follows, with emphasis added:

> Each of the various memory arrays 18 will include a plurality of memory locations (not shown). The number of memory locations will depend on the circumstances such as the function of the specific memory array. **According to the current SPARC specification each of the memory locations is identified by an address consisting of two elements. The first element is a unique ASI for each memory array which distinguishes one memory array from another. For example, if the memory arrays 18 include an instruction cache and a data cache, then each will have a different ASI.** The second element is an address which identifies an offset into its associated address space which corresponds to a particular memory location. Taken together, the two elements guarantee that each memory location on the IC has a unique address. **The SPARC ASI specification also currently stipulates a data field, a read-strobe, and a write-strobe. Taken together these elements are collectively referred to as the ASI bus protocol of a SPARC microprocessor. The ASI bus standardizes the access of all of the memory arrays without necessitating knowledge of their physical structure.**

As another example, Applicants paragraph [006] at page 7 of Applicants' Specification reads as follows, with emphasis added:

> A system for on-chip testing of embedded memories using Address Space Identifier (ASI) bus in Scalable Processor ARChitecture (SPARC) microprocessors is disclosed. An integrated circuit includes a plurality of memory arrays, Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, and a memory control unit and a memory built-in self-test (MBIST) engine connected to the ASI bus interface

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> logic. Rather than direct access, the MBIST engine utilizes the ASI bus interface logic and the ASI bus to perform memory testing. The MBIST engine, programmed with memory array parameters, includes a programmable state machine controller to which is connected a programmable data generator, a programmable address generator, and a programmable comparator. The data generator provides data as appropriate. The address generator provides addresses as appropriate. The comparator provides test results information for the particular test situation. The MBIST engine generates a test status output. Depending on the specific memory array to be tested, the appropriate parameters of that memory array are programmed to configure the MBIST engine to test that memory array.

Numerous other examples of discussions directed to an **Address Space Identifier (ASI) bus** and an **Address Space Identifier (ASI) bus interface logic** structure recited in Applicants' claims are found through out Applicants' specification.

In contrast, the terms Address Space Identifier (ASI) bus and Address Space Identifier (ASI) bus interface logic, or even ASI, are found nowhere in the Irrinki reference, or in any of the Irrinki reference figures. Consequently, Applicants respectfully submit that the Examiner has failed to show where in the Irrinki reference it is disclosed, taught or suggested either an **Address Space Identifier (ASI) bus** or an **Address Space Identifier (ASI) bus interface logic** structure.

In light of the discussion above, Applicants respectfully request the Examiner withdraw the rejection of Claims 1, 12, and 16, as well as dependent Claims 4, 5, 6, 13, 14, 15, 17, 18, and 19, under 35 U.S.C. 102(b) as anticipated by the Irrinki reference (US 6,067,262) and allow Claims 1, 12, and 16, as well as dependent Claims 4, 5, 6, 13, 14, 15, 17, 18, and 19, to issue.

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REJECTION OF CLAIMS 2, 3, 7, 8, 9, 10, and 11 BASED ON 35 U.S.C. 103(a)

The Examiner rejected Claims 2, 3, 7, 8, 9, 10, and 11 under 35 U.S.C. 103(a) as obvious over the Irrinki reference (US 6,067,262) in view of the Dreibelbis et al. reference (US 5,173,906).

Applicants' Claim 1 reads as follows, with emphasis added:

> An integrated circuit comprising:
> a plurality of memory arrays;
> **Address Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, wherein the **ASI bus interface logic controls access to the plurality of memory arrays**;
> a memory control unit connected to the **ASI bus interface logic**; and
> a memory built-in self-test (MBIST) engine connected to **the ASI bus interface logic**, wherein the MBIST engine utilizes **the ASI bus interface logic** to perform memory testing on at least one of the plurality of memory arrays.

Applicants' Claim 7 reads as follows, with emphasis added:

> A memory built-in self-test (MBIST) engine for an integrated circuit having a plurality of memory arrays, **Address Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, and a memory control unit connected to **the ASI bus interface logic**, wherein the MBIST engine utilizes **the ASI bus interface logic** to perform memory testing on at least one of the plurality of memory arrays, the MBIST engine comprising:
> a programmable state machine controller;
> a programmable data generator connected to the controller, wherein the data generator provides data appropriate for a particular test situation;
> a programmable address generator connected to the controller, wherein the address generator

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provides addresses appropriate for the particular test situation; and

a programmable comparator connected to the controller, wherein the comparator provides test results information for the particular test situation to the controller.

Applicants' Claim 12 reads as follows, with emphasis added:

A method of memory built-in self-test (MBIST) for an integrated circuit having a plurality of memory arrays, Address **Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, a memory control unit connected to **the ASI bus interface logic**, and an MBIST engine connected to **the ASI bus interface logic**, the method comprising:

utilizing **the ASI bus interface logic** to perform memory testing on at least one of the plurality of memory arrays.

Applicants' Claim 16 reads as follows, with emphasis added:

An apparatus for memory built-in self-test (MBIST) for an integrated circuit having a plurality of memory arrays, **Address Space Identifier (ASI) bus interface logic** connected by **an ASI bus** to the plurality of memory arrays, a memory control unit connected to **the ASI bus interface logic**, and an MBIST engine connected to **the ASI bus interface logic**, the apparatus comprising:

means for utilizing the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays.

As shown above, each of Applicants' independent Claims specifically recites, multiple times per claim, an **Address Space Identifier (ASI) bus** and **Address Space Identifier (ASI) bus interface logic.**

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> is an address which identifies an offset into its associated address space which corresponds to a particular memory location. Taken together, the two elements guarantee that each memory location on the IC has a unique address. **The SPARC ASI specification also currently stipulates a data field, a read-strobe, and a write-strobe. Taken together these elements are collectively referred to as the ASI bus protocol of a SPARC microprocessor. The ASI bus standardizes the access of all of the memory arrays without necessitating knowledge of their physical structure.**

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In contrast, the terms Address Space Identifier (ASI) bus and Address Space Identifier (ASI) bus interface logic, or even ASI, are found nowhere in the Irrinki reference, or in any of the Irrinki reference figures. Consequently, Applicants respectfully submit that the Examiner has failed to show where in the Irrinki reference it is disclosed, taught or suggested either an **Address Space Identifier (ASI) bus** or an **Address Space Identifier (ASI) bus interface logic** structure.

In light of the discussion above, Applicants respectfully submit that Claims 1, 12, 7, and 16 are patentable over the Irrinki reference.

The addition of the Dreibelbis et al. reference (US 5,173,906) does nothing to cure the basic deficiency of the Irrinki reference discussed above. Consequently Applicants respectfully submit that Claims 1, 12, 7, and 16 are patentable over the Irrinki reference, the Dreibelbis et al. reference, or any proper combination of the Irrinki reference and the Dreibelbis et al. reference for at least the reasons discussed above.

In light of the discussion above, Applicants respectfully request the Examiner withdraw the rejection of Claim 7 under 35 U.S.C. 103(a) as obvious over the Irrinki reference (US 6,067,262) in view of the Dreibelbis et al. reference (US 5,173,906) and allow Claim 7 to issue.

Claims 2 and 3 depend, directly or indirectly on Claim 1. Claims 8, 9, 10 and 11 depend, directly or indirectly on Claim 7. Consequently, In light of the discussion above, Applicants respectfully request the Examiner withdraw the rejection of Claims 2, 3, 8, 9, 10 and 11 under 35 U.S.C. 103(a) as obvious

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over the Irrinki reference (US 6,067,262) in view of the Dreibelbis et al. reference (US 5,173,906) and allow Claims 2, 3, 8, 9, 10 and 11 to issue as well.

CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 10, 2006.

Attorney for Applicant(s) — April 10, 2006 Date of Signature

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